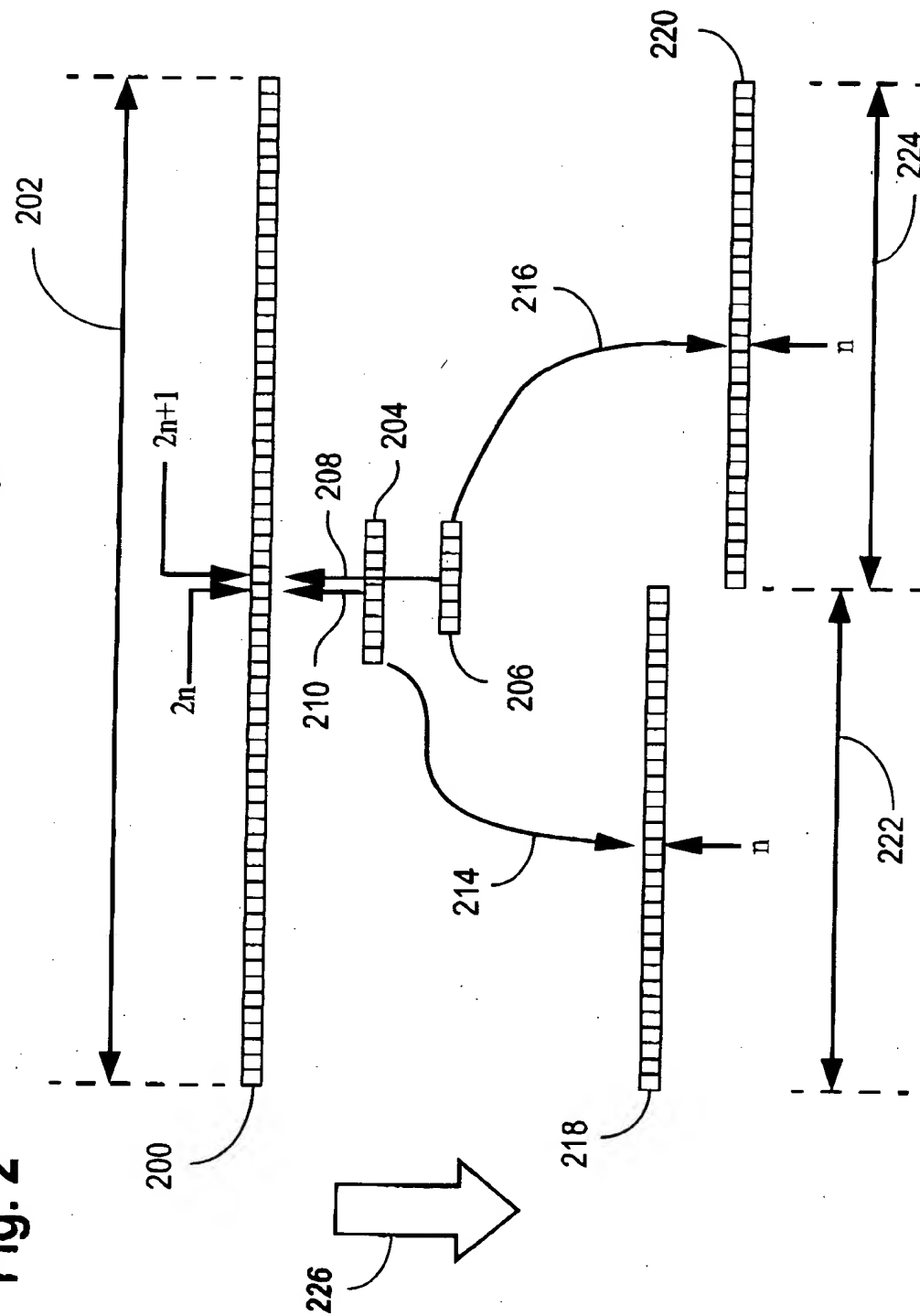


Fig. 1

212



308

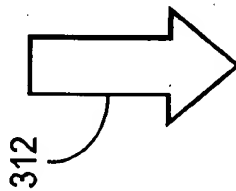
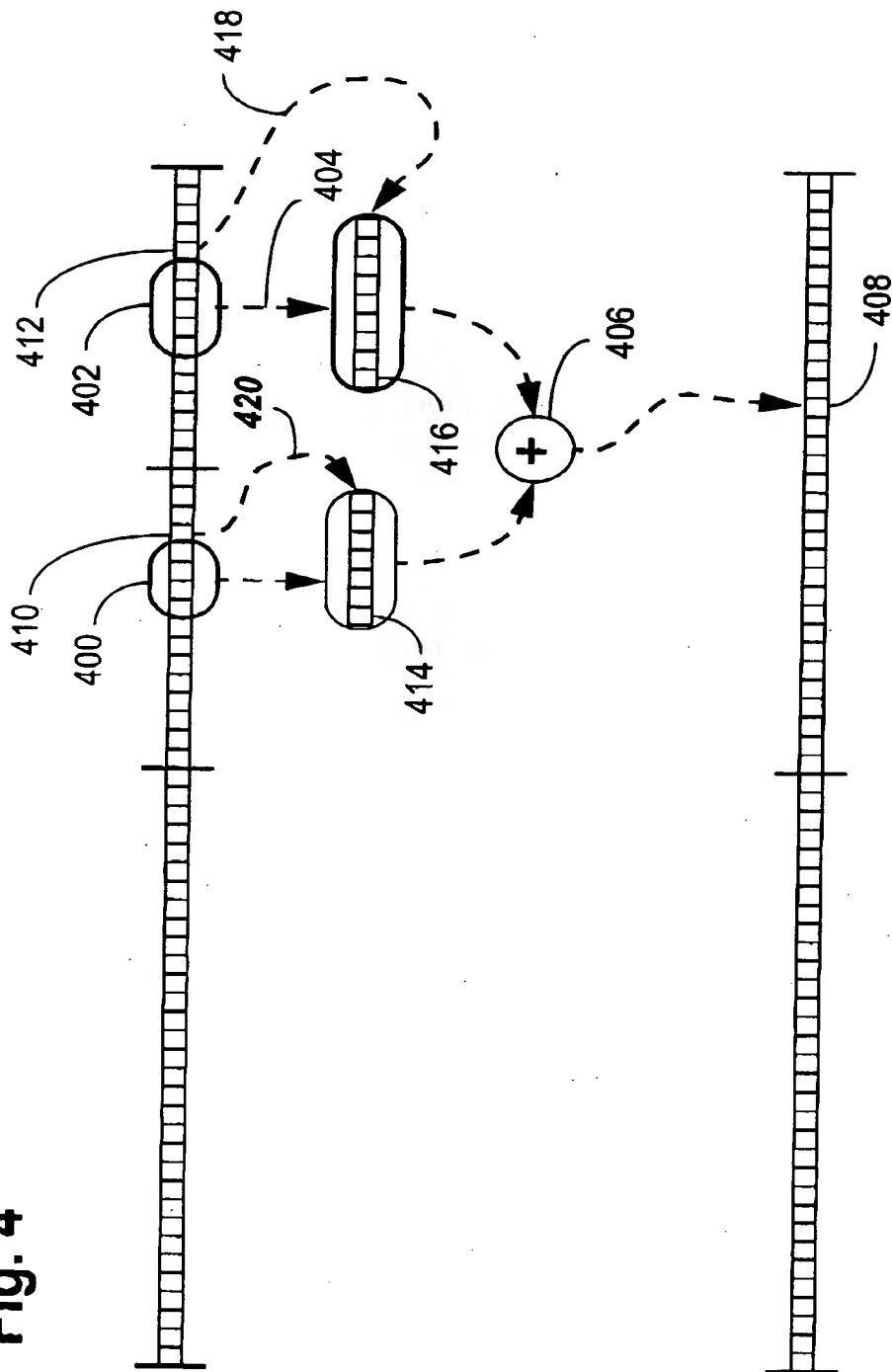


Fig. 4



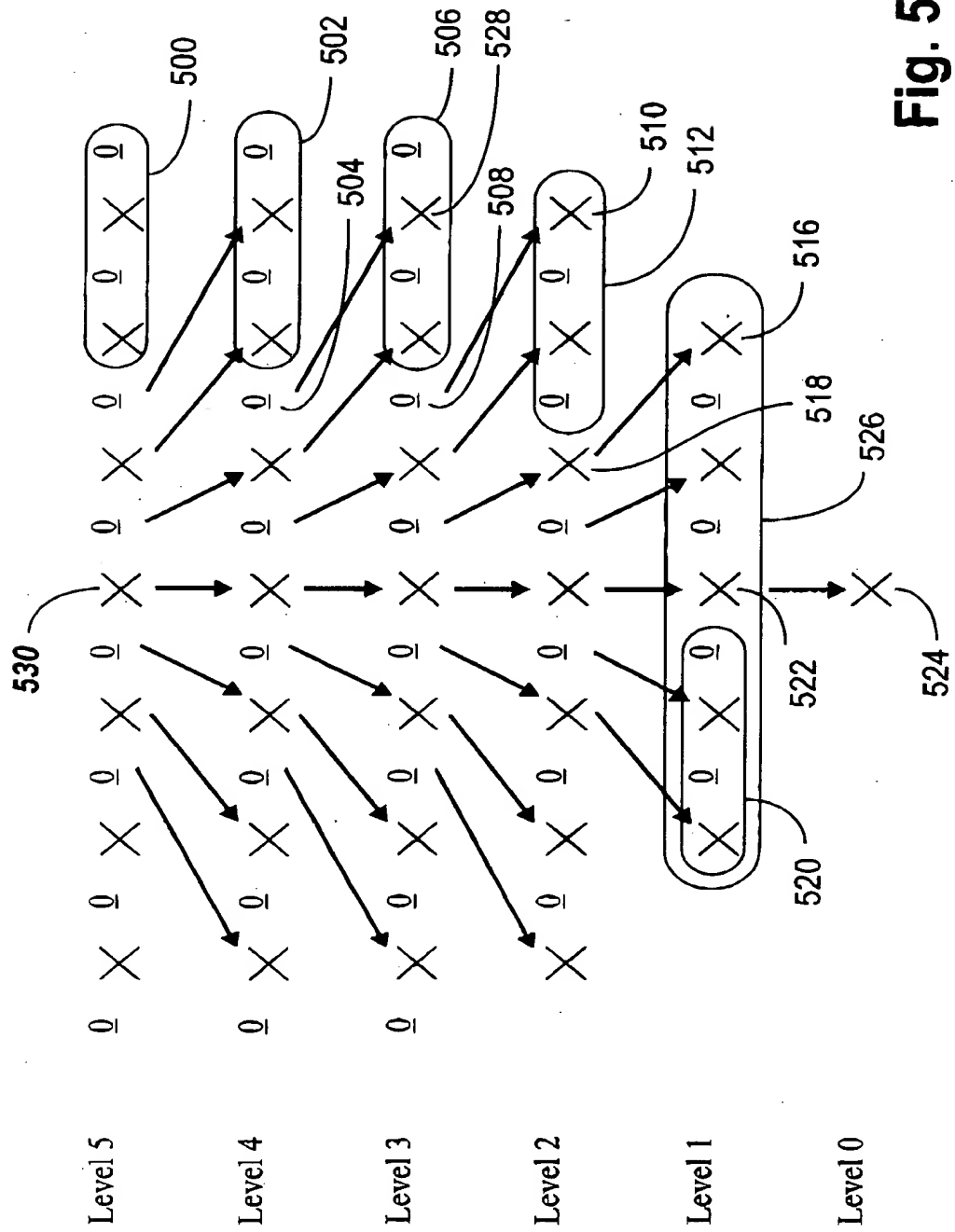


Fig. 5

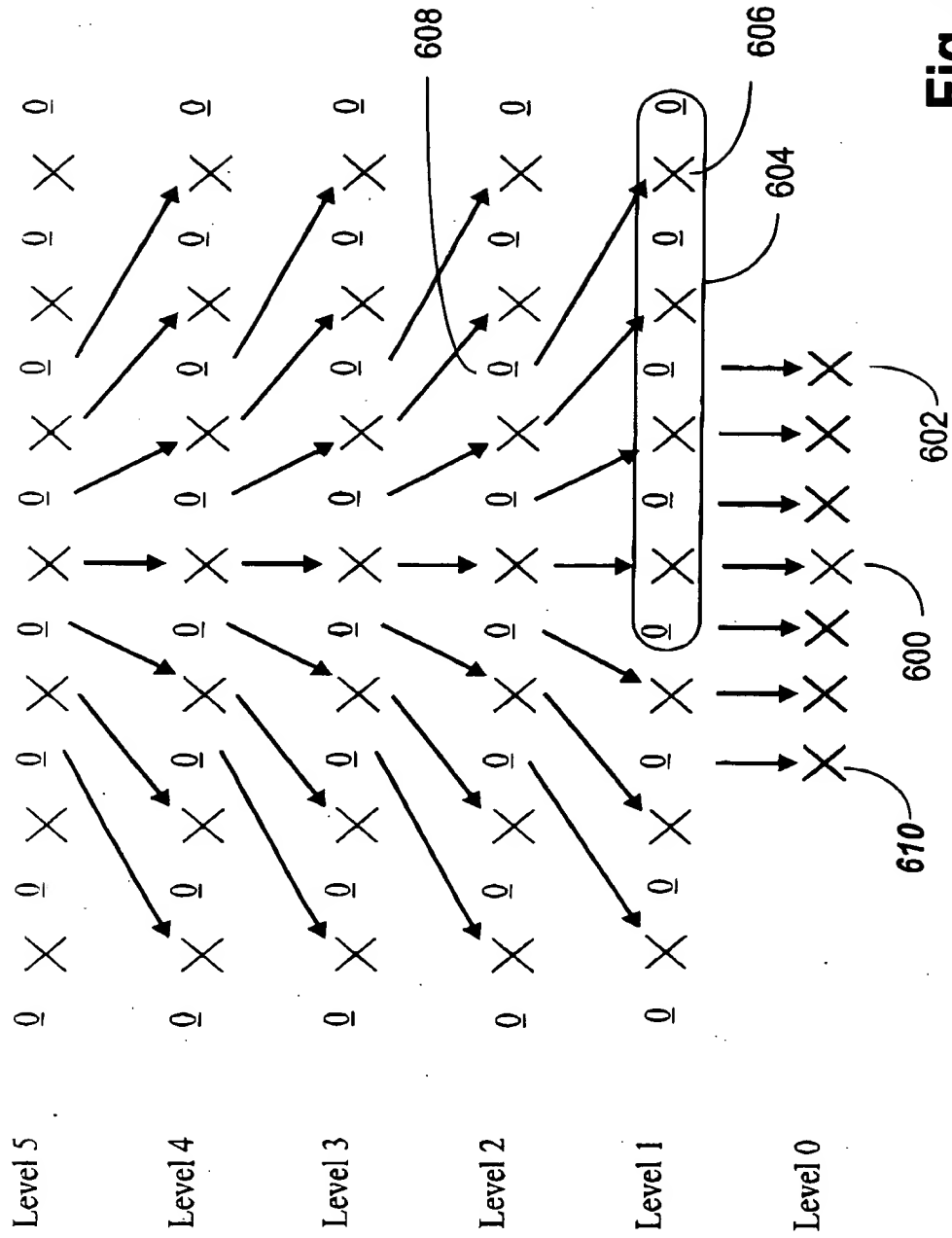


Fig. 6

7/23

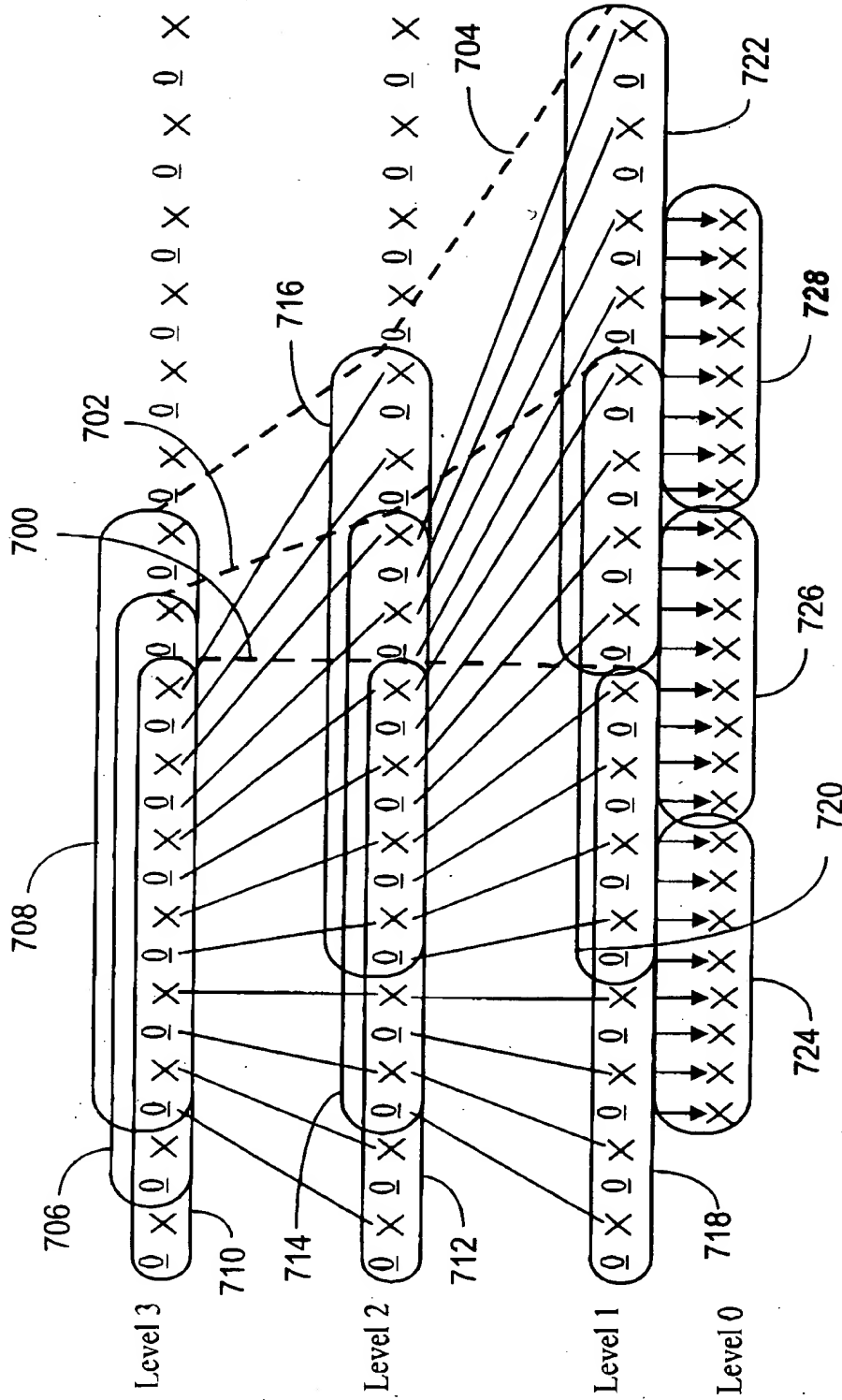


Fig. 7

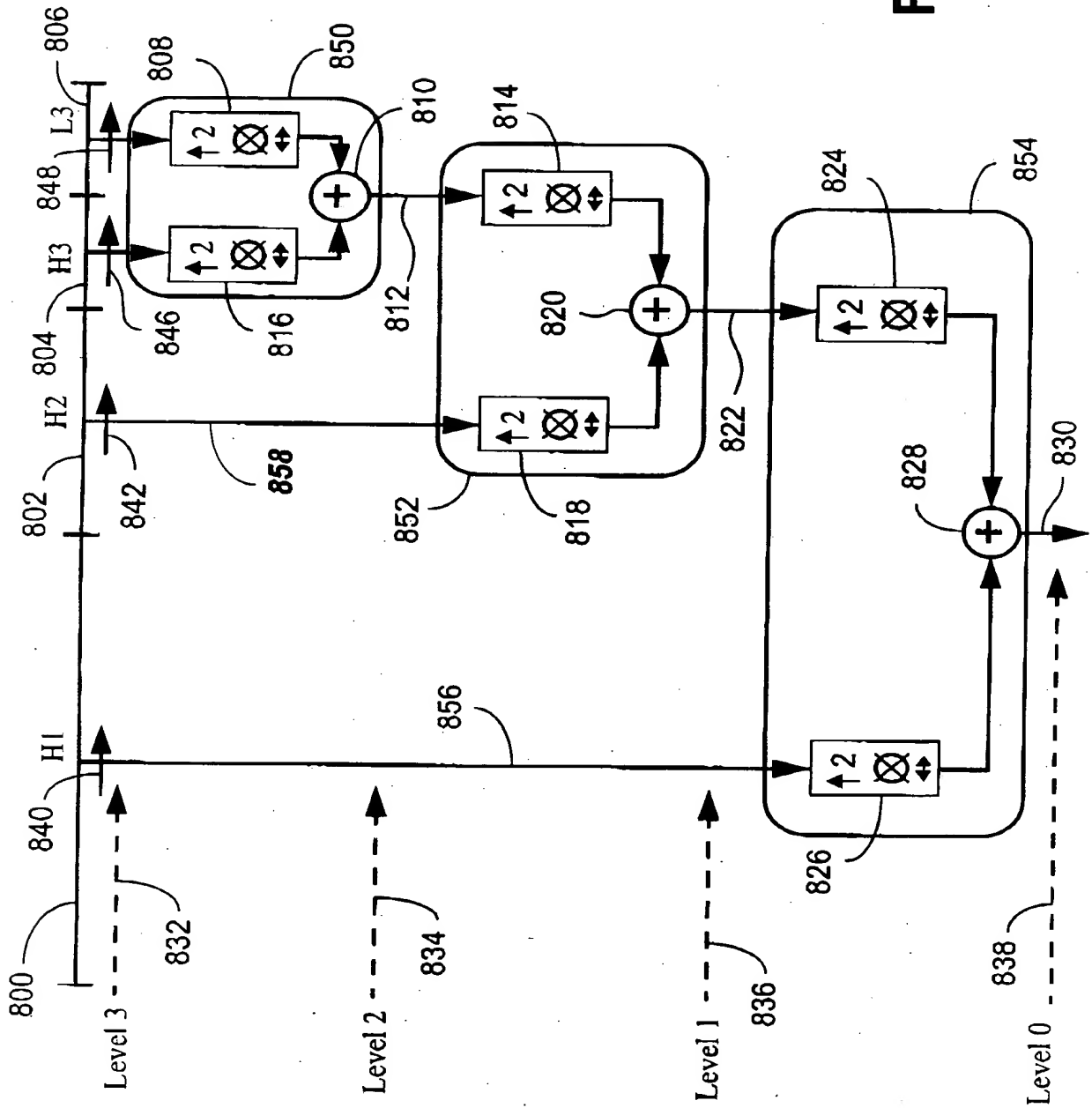
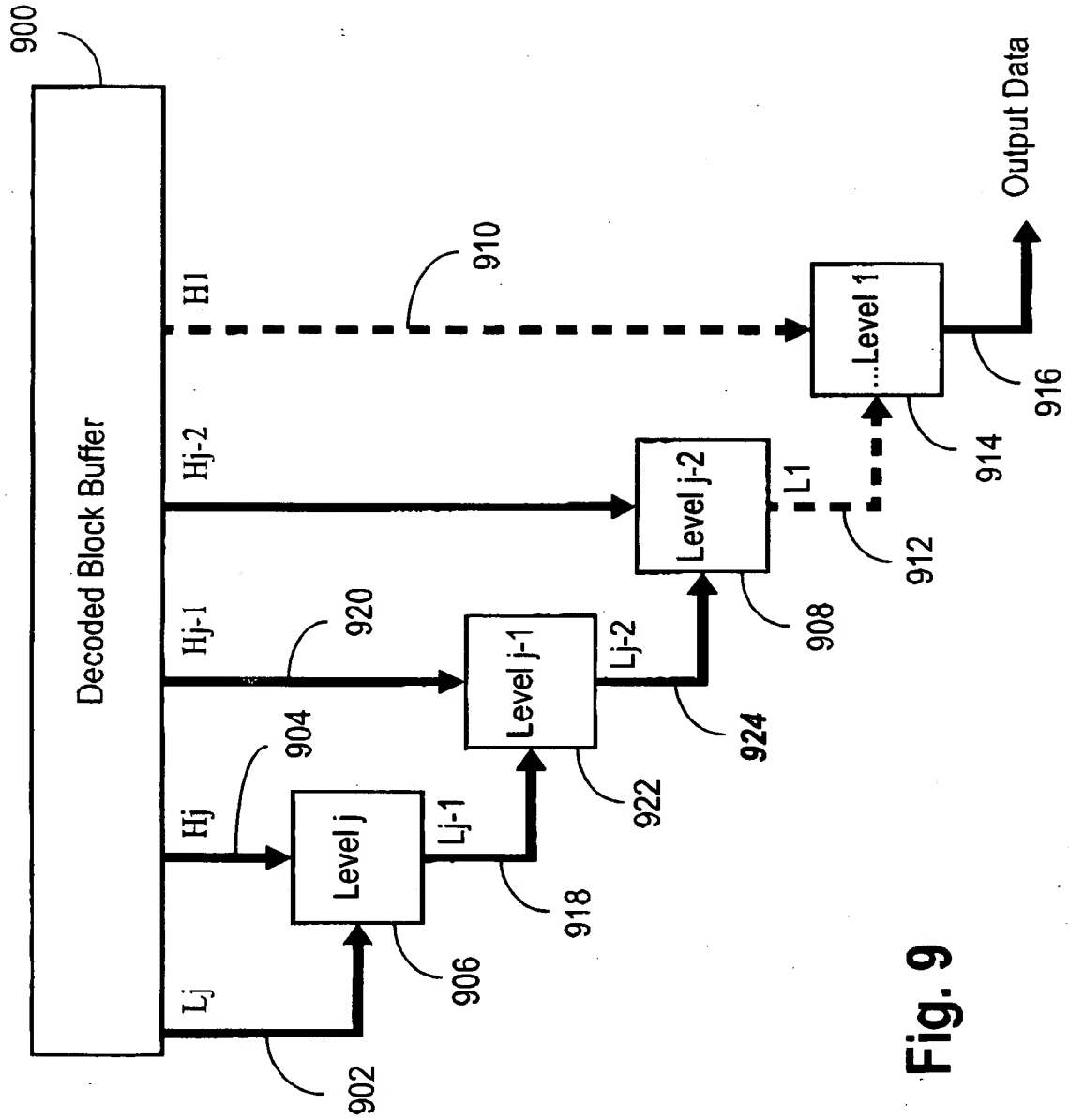


Fig. 8



00/02 F" 2550E/50

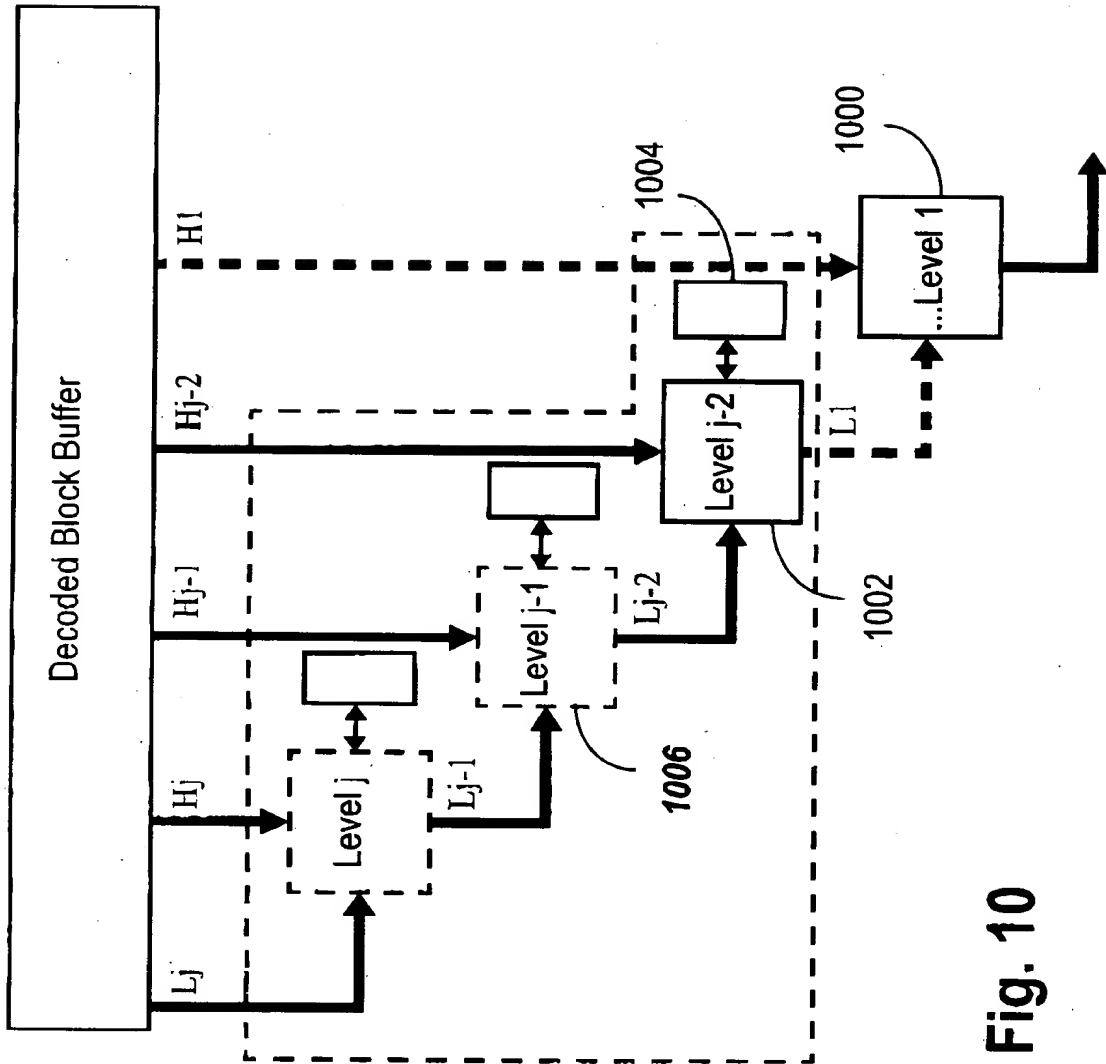


Fig. 10

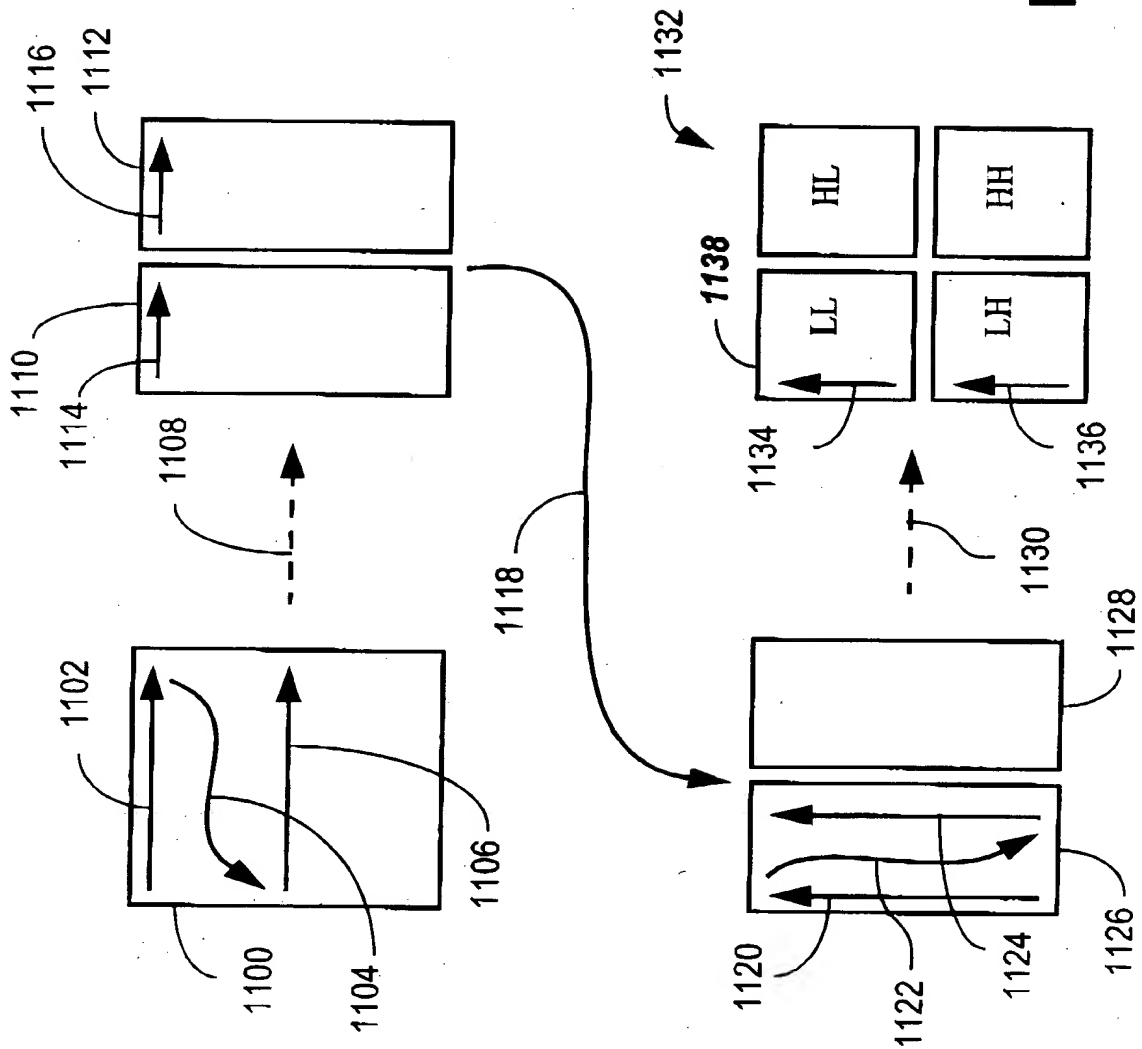


Fig. 11

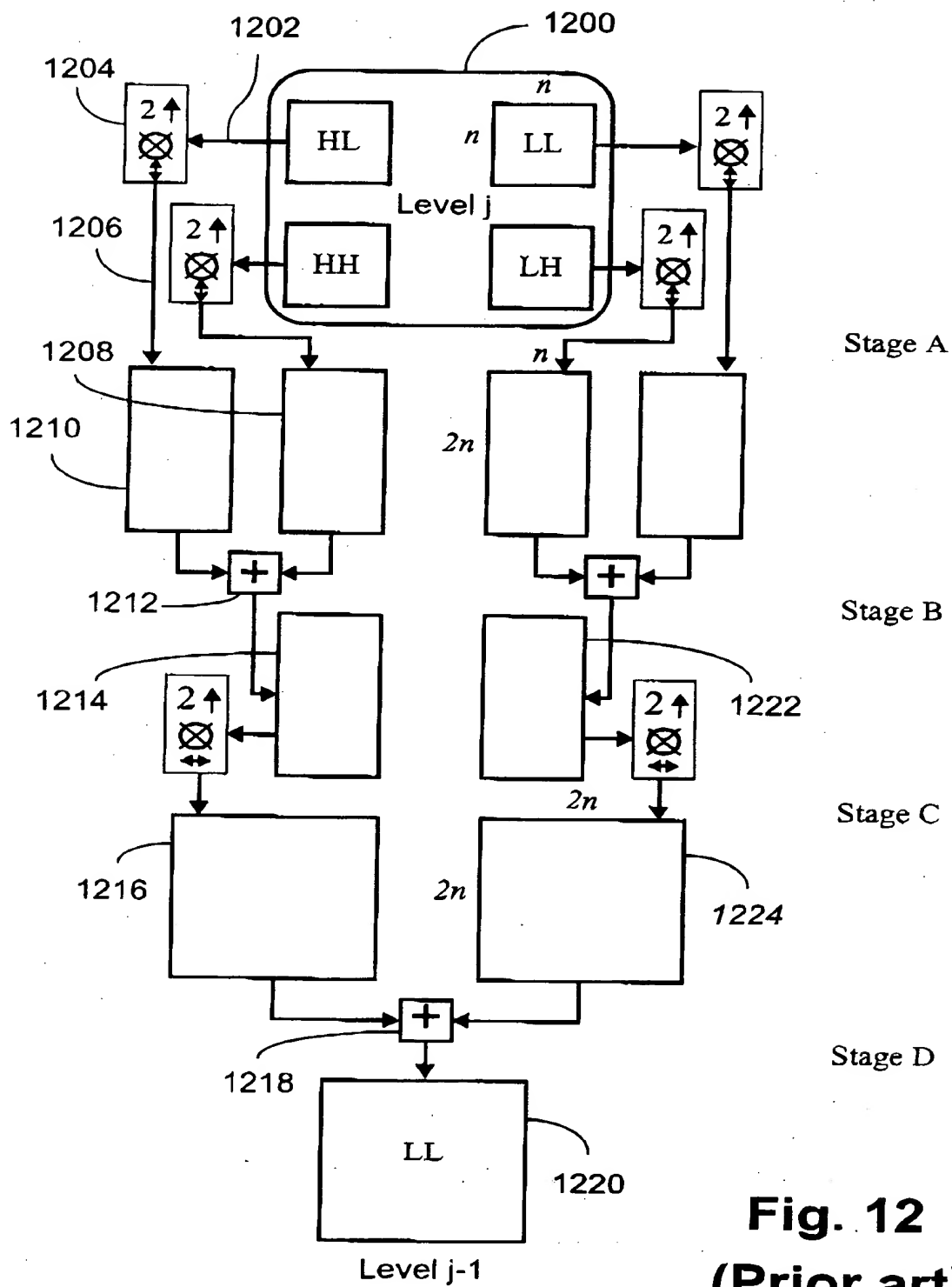


Fig. 12
(Prior art)

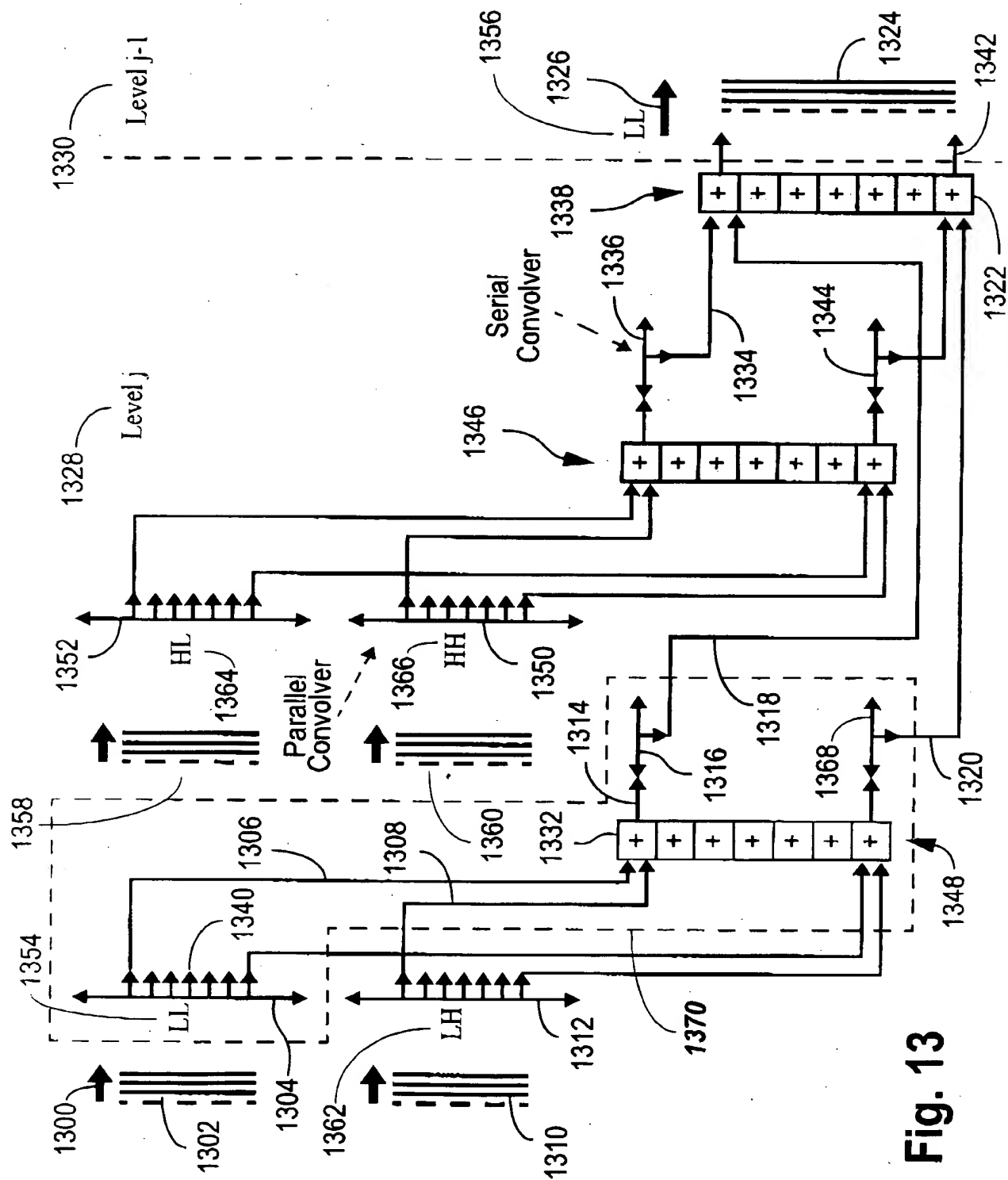
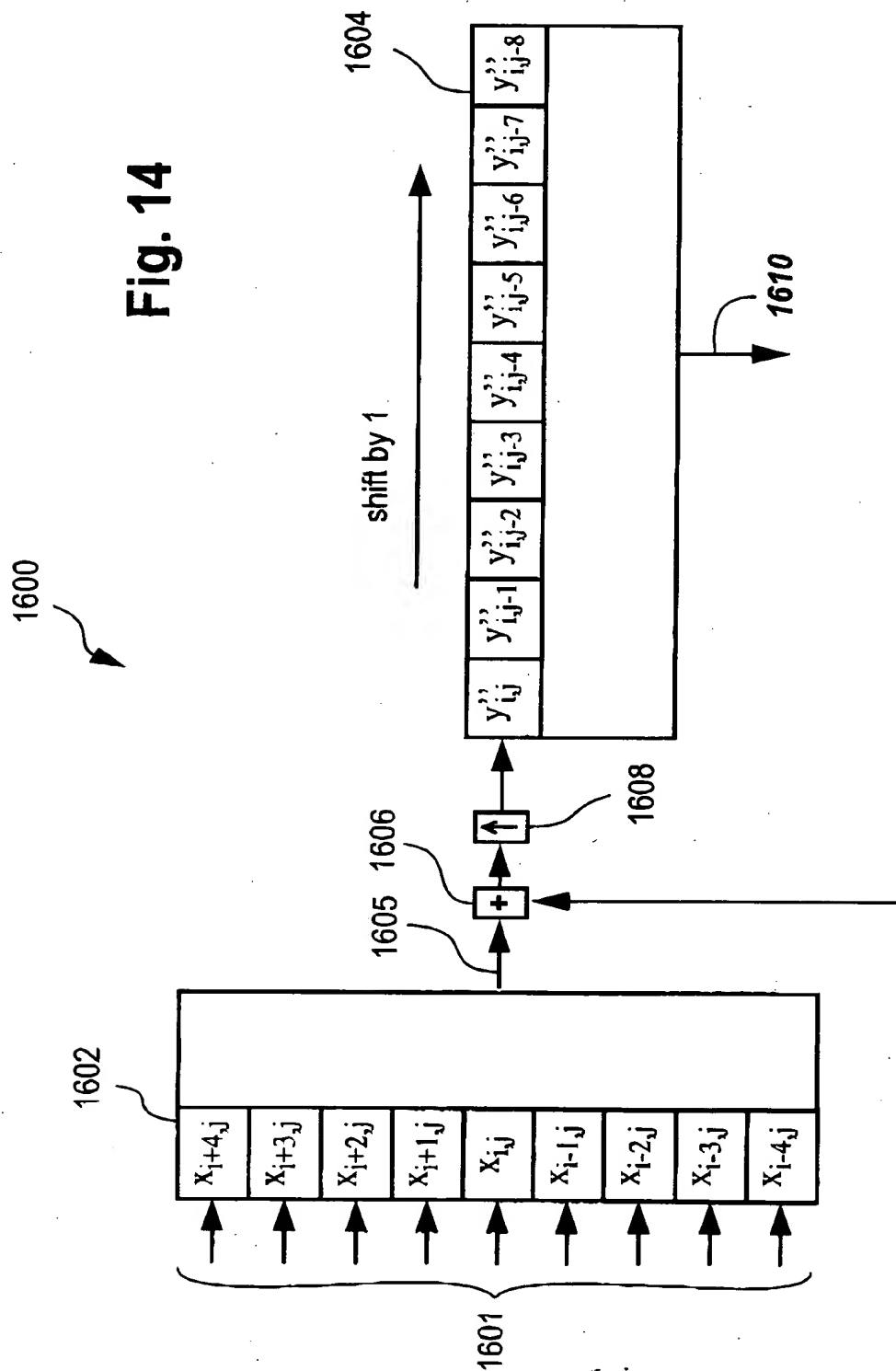


Fig. 13

Fig. 14



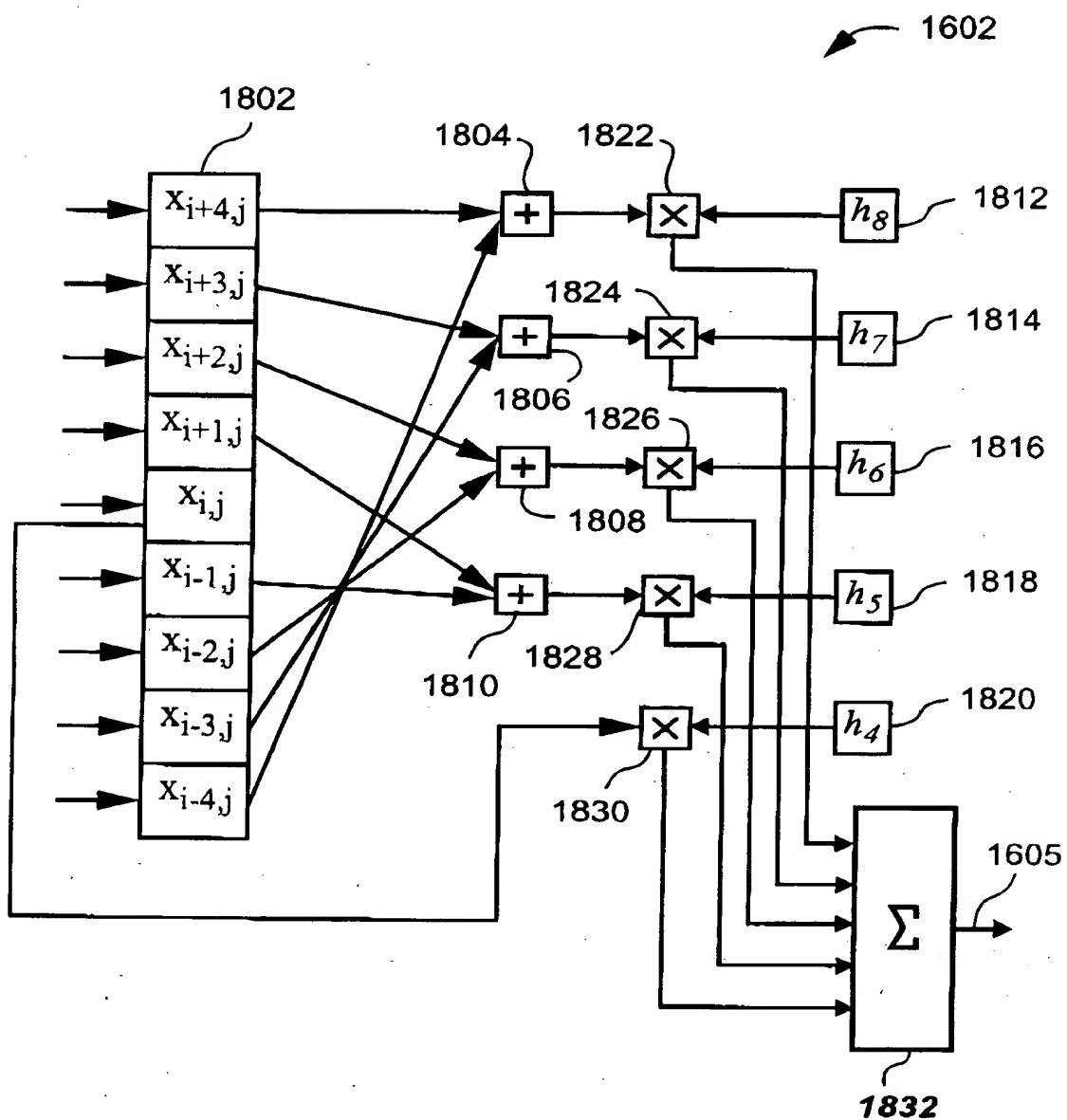


Fig. 15

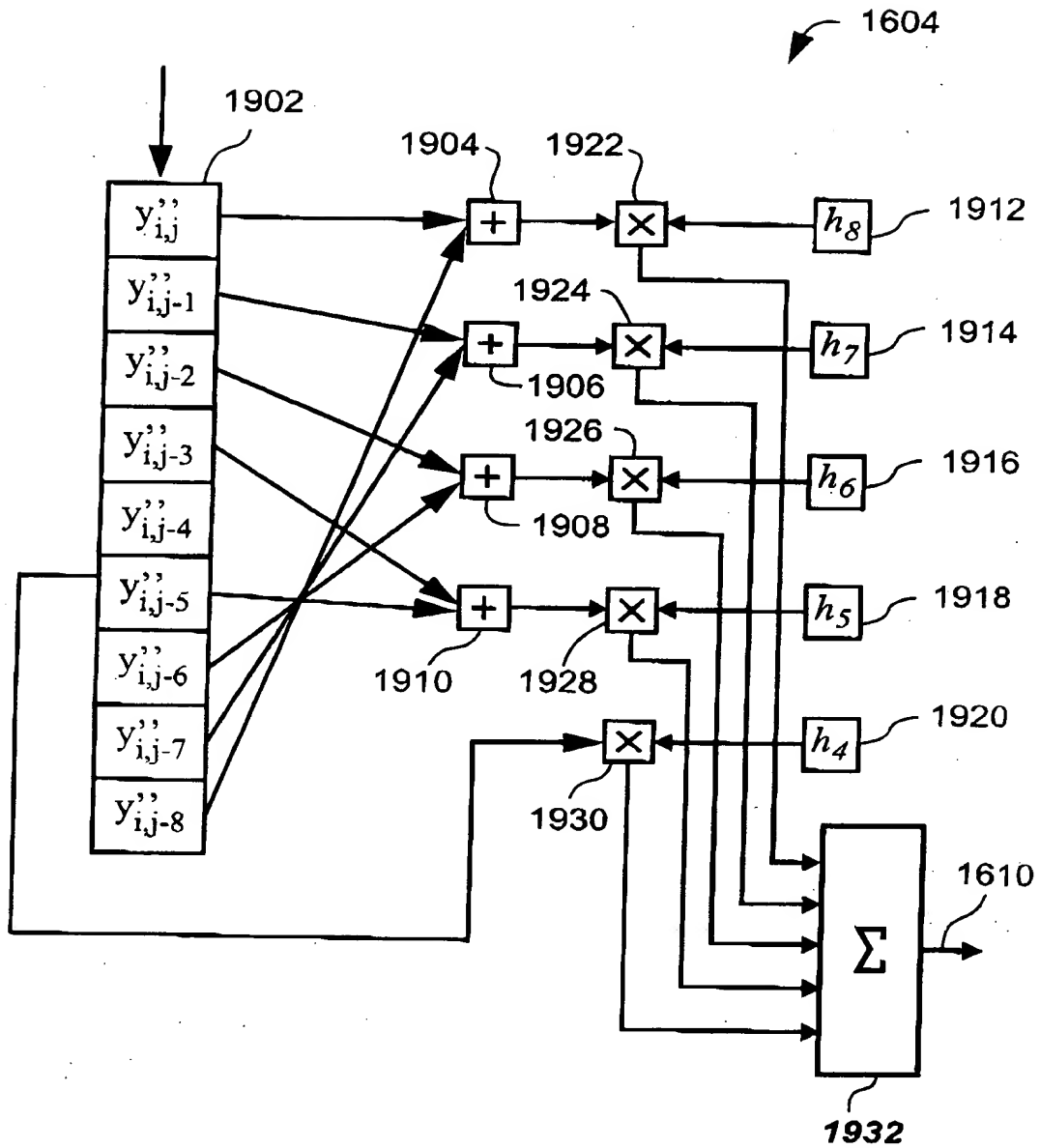
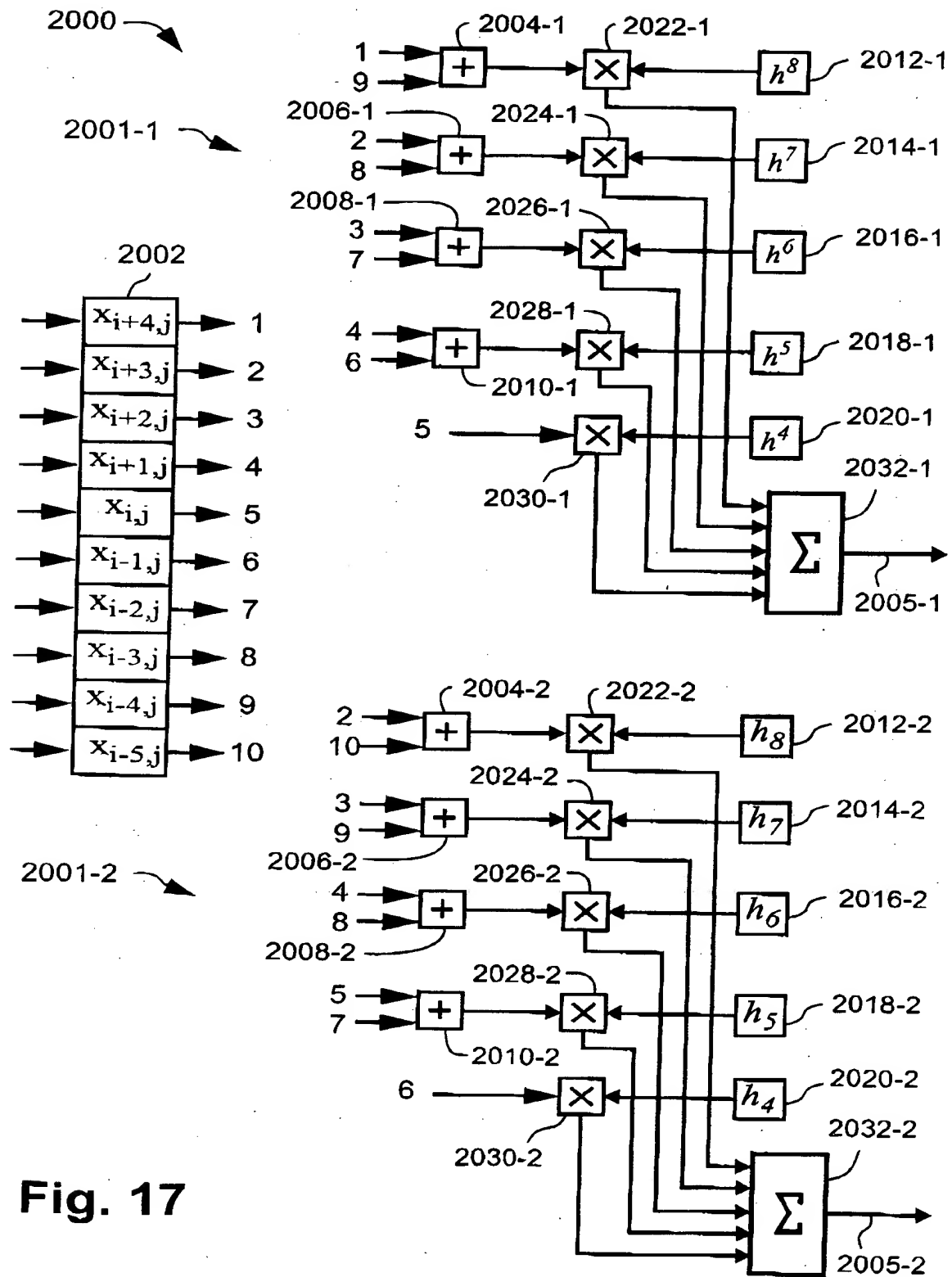
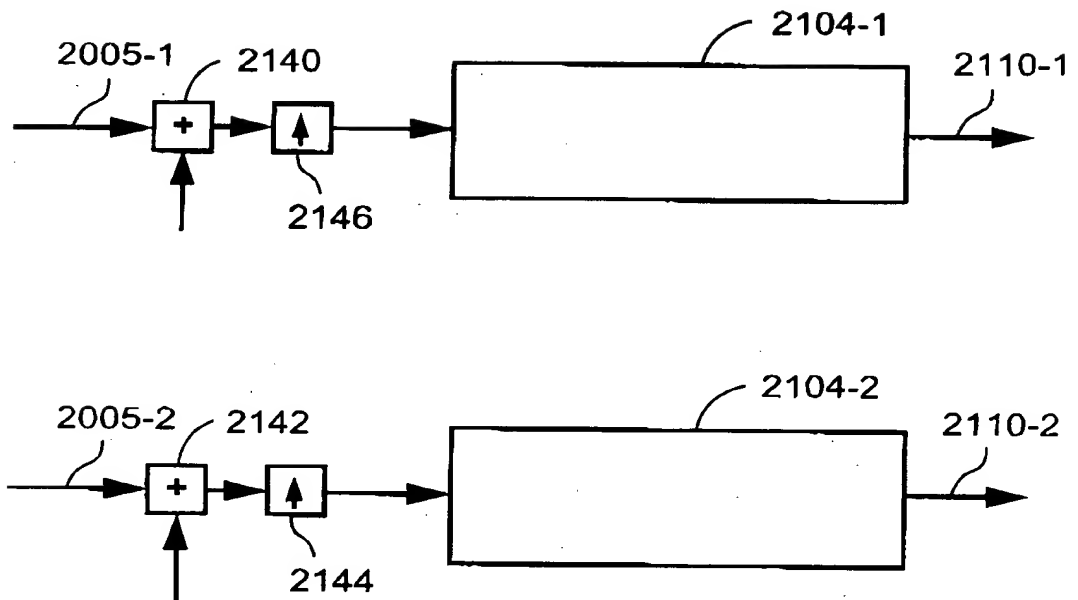
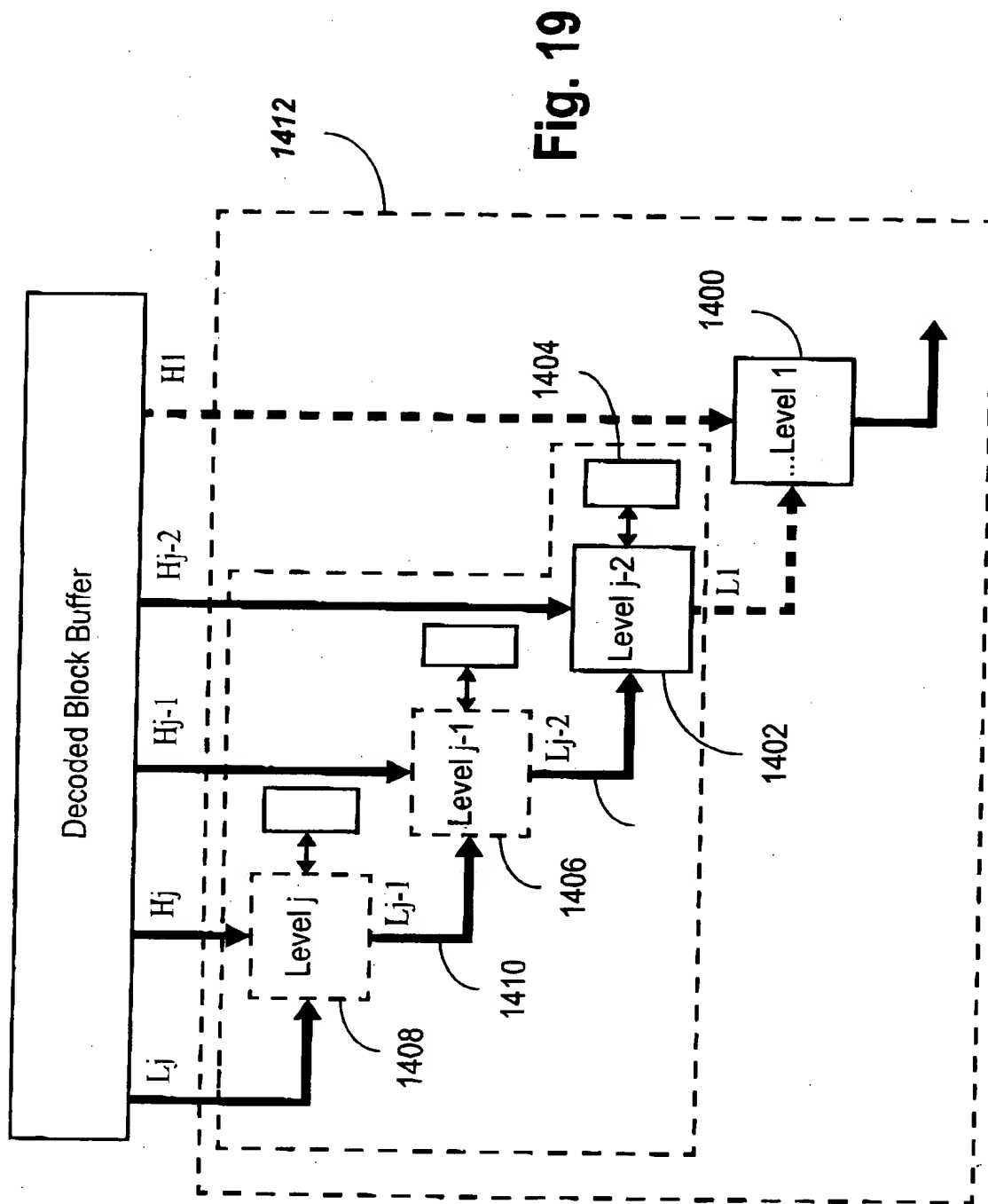


Fig. 16



2100

**Fig. 18**



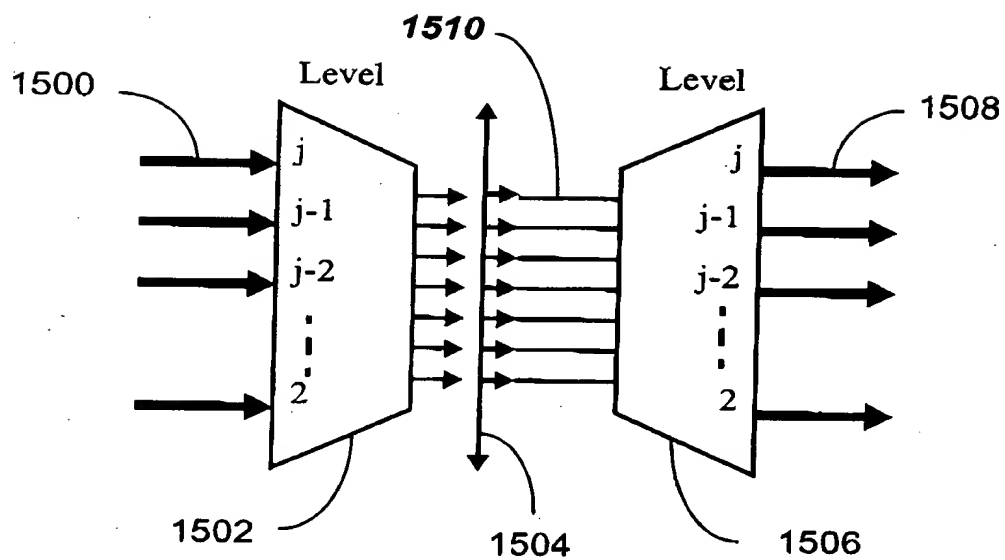
**Fig. 20**

Fig. 21

Stage 1

2200

Level j

Level j-1

Level k+1

output buffer

2204

Stage 2

2206

Level k

Level k-1

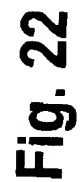
Level 1

output buffer

2208

output data

Logical mapping of next stage onto same computational pipeline.



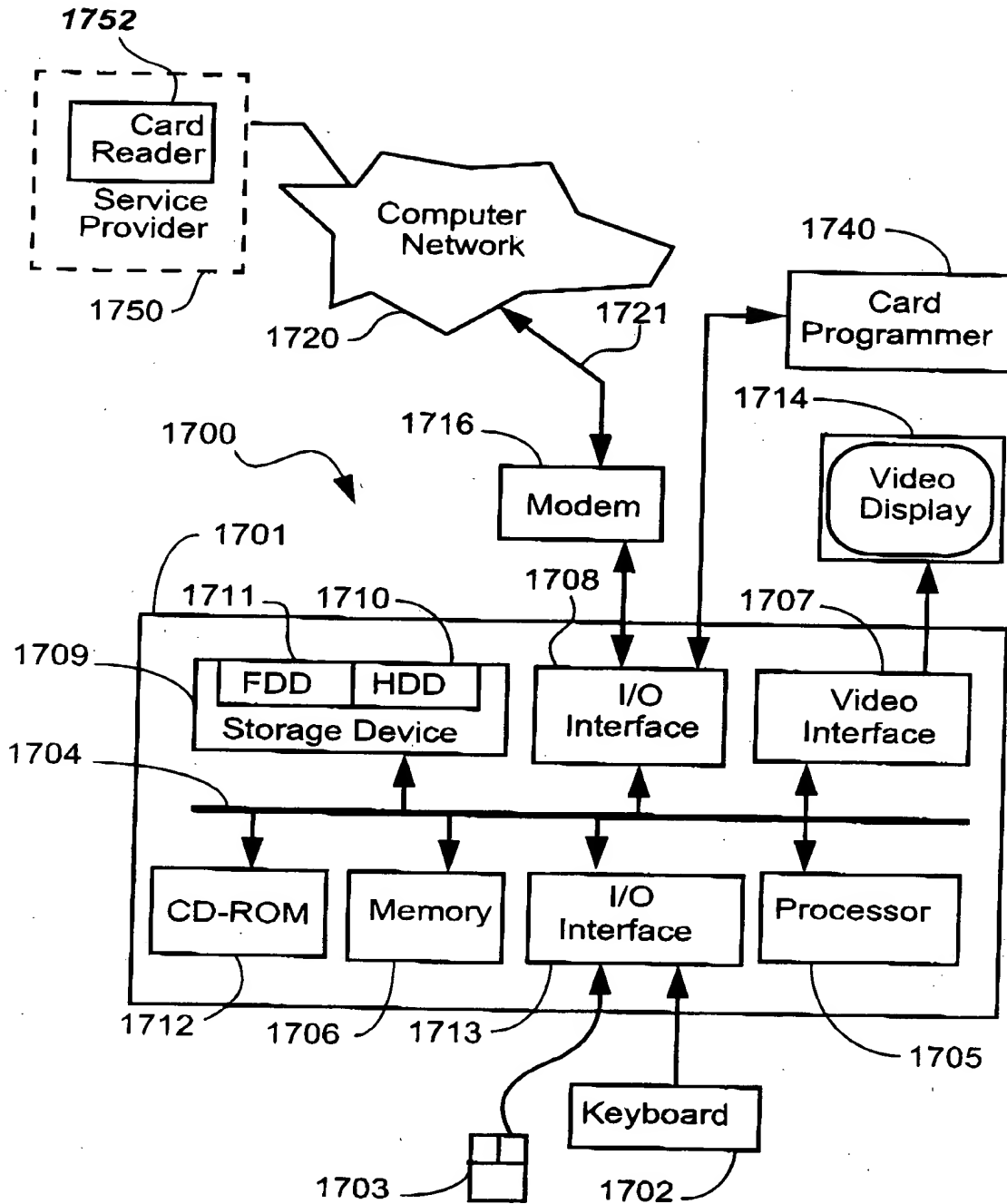


Fig. 23